

CLAIMS

What is claimed is:

- 1 1. A method for fabricating a bipolar transistor comprising:
2 forming an emitter region in a first epitaxial layer;
3 etching the first epitaxial layer using an emitter pedestal structure
4 as a masking member;
5 growing a second epitaxial layer on the first epitaxial layer.
- 1 2. The method defined by claim 1, wherein the etching includes
2 isotropic etching so as to undercut the emitter pedestal structure.
- 1 3. The method defined by claim 2, wherein a second epitaxial layer is
2 more heavily doped than the first epitaxial layer.
- 1 4. The method defined by claim 1, including:
2 forming a polysilicon layer on an oxide layer having an opening
3 which exposes the emitter region;
4 defining an emitter pedestal from the polysilicon layer; and
5 forming oxide sidewall spacers on the emitter pedestal.
- 1 5. The method defined by claim 4, wherein the first epitaxial layer is a
2 silicon-germanium layer.
- 1 6. The method defined by claim 5, wherein the second epitaxial layer
2 is a silicon-germanium layer.
- 1 7. A method for fabricating a bipolar transistor comprising:
2 forming a first epitaxial layer over a collector region;

3 forming an emitter region in the first epitaxial layer and an emitter
4 pedestal above the first epitaxial layer;
5 forming sidewall spacers on the emitter pedestal over the first
6 epitaxial layer;
7 etching the first epitaxial layer including undercutting the sidewall
8 spacers; and
9 growing a second epitaxial layer on the first epitaxial layer.

1 8. The method defined by claim 7, wherein the first and second
2 epitaxial layers are doped with a first conductivity type dopant.

1 9. The method defined by claim 8, wherein the second epitaxial layer
2 is doped more heavily than the first epitaxial layer with the first
3 conductivity type dopant.

1 10. The method defined by claim 9, wherein the second epitaxial layer
2 is grown to a level above an upper level of the first epitaxial layer.

1 11. The method defined by claim 9, wherein the first and second
2 epitaxial layers comprise silicon-germanium.

1 12. The method defined by claim 7, wherein the emitter pedestal is
2 formed from a polysilicon layer doped with a second conductivity type
3 dopant.

1 13. The method defined by claim 12, wherein the formation of the
2 emitter region and emitter pedestal includes:

3 forming an oxide layer on the first epitaxial layer;

4 defining an opening in the oxide layer for the emitter region;
5 forming the polysilicon layer over the oxide layer; and
6 driving the second conductivity type dopant from the polysilicon
7 layer into the first epitaxial layer to define the emitter region.

1 14. The method defined by claim 7, wherein the etching comprises use
2 of an isotropic etchant.

1 15. The method of claim 7, wherein the first epitaxial layer includes the
2 intrinsic base region and at least part of the link based region for the
3 transistor.

1 16. The method defined by claim 15, wherein the second epitaxial layer
2 comprises the extrinsic base region for the transistor.

1 17. A bipolar transistor comprising:
2 a monocrystalline extrinsic base region having relatively vertical
3 sidewalls adjacent a monocrystalline link base region, the extrinsic base
4 region being more heavily doped than the adjacent link base region.

1 18. The transistor defined by claim 17, wherein the extrinsic base
2 region is doped to a level 10 times or greater than the doping level in the
3 adjacent link base region.

1 19. The transistor of claim 17, including an emitter pedestal structure
2 having, an emitter pedestal, sidewall spacers on the sides of the pedestal,
3 and oxide regions under the pedestal having an opening communicating

4 with an emitter region of the transistor, wherein the extrinsic base region
5 extends under the spacers.

1 20. The transistor defined by claim 17, wherein the monocrystalline
2 extrinsic base region is disposed on an underlying monocrystalline layer
3 having the link base region and an intrinsic base region for the transistor.

1 21. The transistor defined by claim 20, wherein the monocrystalline
2 extrinsic base region is doped to a level 10 times or greater than the
3 doping level in the adjacent link base region.

1 22. The transistor defined by claim 21, wherein the extrinsic base
2 region and underlying monocrystalline layer are silicon-germanium.